ERD-01-001

February 6, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/016,915 12/14/01

David Meltzer

A LOCK DETECTOR CIRCUIT FOR DEJITTER PHASE LOCK LOOP (PLL) APPLICATIONS

Grp. Art Unit: 2631

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 15, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date SBA 2/15/02

The structure of a phase lock loop is well known in the art as shown in "Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs," Nayan Patel, SCAA033A, Texas Instruments, March 1997, and "Phase-Locked Loops for High-Frequency Receivers and Transmitters - Part 1," Curtin and O'Brian, Analog Dialogue, 33-3, 1999.

The TQ8103 Clock & Data Recovery (CDR) product description discloses a monolithic CDR IC manufactured by Triquint Semiconductor Inc., which receives NRZ data, extracts the high-speed clock and presents separated data and clock as outputs.

The AMCC S3040A Device Specification (April 2, 2000) describes a clock recovery unit used to device high speed timing signals for SONET/SDH-based equipment.

U.S. Patent 6,215,834 to McCollough, "Dual Bandwidth Phase Locked Loop Frequency Lock Detection System and Method," discloses a frequency lock detector for a dual bandwidth PLL.

U.S. Patent 5,963,608 to Casper et al., "Clock Extractor for High Speed Variable Data Rate Communication System," discloses a data rate estimator-based, variable data rate synchronizer that extracts a clock signal embedded within a digital data signal.

U.S. Patent 5,886,582 to Stansell, "Enabling Clock Sgnals with a Phase Locked Loop (PLL) Lock Detect Circuit," discloses a circuit for enabling and disabling generation of an output clock signal.

U.S. Patent 5,870,002 to Ghaderi et al., "Phase-Frequency Lock Detector," discloses a method and circuitry for detecting when a PLL achieves phase and frequency-lock to a reference frequency with minimal hardware and power dissipation.

U.S. Patent 5,838,749 to Casper et al., "Method and Apparatus for Extracting an Embedded Clock from a Digital Data Signal," discloses a high speed, wide data rate range (e.g. 10-300 Mb/s), fiber optic digital communication system.

U.S. Patent 5,822,387 to Mar, "Apparatus for Fast Phase-Locked Loop (PLL) Frequency Slewing During Power On," discloses a clock synthesizer that includes a phase-locked loop circuit having two modes of operation: a non-slewing mode of operation, and a feequency-slewing mode of operation.

U.S. Patent 5,724,007 to Mar, "Adjustable Lock Detector for a Phase-Locked Loop Circuit," discloses a lock detector suitable for detecting when an output signal of a phase-locked loop circuit is phase-locked to an input reference signal.

U.S. Patent 5,394,444 to Silvey et al., "Lock Detect Circuit for Detecting a Lock Condition in a Phase Locked Loop and Method Therefor," discloses a lock detect circuit for detecting a lock condition in a phased lock loop.

U.S. Patent 4,499,434 to Thompson, "PLL Phase Error Alarm Related to Associated Receiver," discloses improvements in error alarms used in conjunction with phase locked signal sources for use in phase modulated communication systems.

U.S. Patent 5,359,727 to Kurita et al., "Clock Generator Using PLL and Information Processing System Using the Clock Generator," discloses a clock generation circuit for a semiconductor integrated circuit device including an information processing system in which logic operations are carried out based upon the clock.

U.S. Patent 5,463,329 to Kawasaki et al., "Input Circuit for Level-Shifting TTL or CMOS to ECL Signals," discloses an input circuit which converts an input signal to an output signal.

U.S. Patent 5,382,923 to Shimada et al., "Charge-Pump Circuit for Use in Phase Locked Loop," discloses a charge-pump circuit for controlling a voltage controlled oscillator by converting a phase difference between two input signals, which never become low at the same time, into a voltage.

U.S. Patent 5,570,042 to Ma, "PECL Input Buffer," discloses an input buffer utilized to first amplify a differential clock or data signal pair to a desired voltage level before being presented to a CMOS or NMOS differential amplifier.

U.S. Patent 5,581,214 to Iga, "Phase-Locked Loop Circuit," discloses a technique for reducing a time required for lock-up of the phase-locked loop circuit which operates intermittently.

U.S. Patent 5,793,225 to Gerson, "CMOS SONET/ATM Receiver Suitable for Use with Pseudo ECL and TTL Signaling Environments," discloses a high-speed pulse receiver.

U.S. Patent 5,905,386 to Gerson, "CMOS SONET/ATM Receiver Suitabale for Use with Pseudo ECL and TTL Signaling Environments," discloses a high-speed pulse receiver.

U.S. Patent 6,246,294 to Gai, "Supply Noise Immunity Low-Jitter Voltage-Controlled Oscillator Design," discloses a phase-locked loop system that generates an output signal having low jitter.

U.S. Patent 6,285,262 to Kuriyama, "Frequency Divider, a Phase Lock Oscillator and a Flip-Flop Circuit Using the Frequency Divider," discloses a frequency divider comprising first and second basic gates.

U.S. Patent 5,614,843 to Mita et al., "CMOS-PECL Level Conversion Circuit," discloses a level conversion circuit which is utilized in a PECL (Pseudo-ECL) interface serving as a small amplitude interface to convert a voltage level from a CMOS level to a PECL level.

U.S. Patent 5,889,437 to Lee, "Frequency Synthesizer with Low Jitter Noise," discloses an improved apparatus for combining frequencies which is capable of generating a constant frequency when an external variation is applied thereto by implementing each block using a differential circuit.

U.S. Patent 6,111,469 to Adachi, "Charge Pumping Circuit and PLL Frequency Synthisizer," discloses a charge pumping circuit including a constant current source, a switch element, a first MOS transistor, a second MOS transistor, and a switching-off circuit.

U.S. Patent 4,736,167 to Kojima et al., "PLL Frequency Synthesizer," discloses a phase locked loop frequency synthesizer.

U.S. Patent 4,818,950 to Ranger, "Low Jitter Phase-Licked Loop," discloses digital phase-locked loops for synchronizing a local clock signal to a received digital signal with minimum jitter.

U.S. Patent 5,151,665 to Wentzler, "Phase-Lock-Loop System with Variable Bandwidth and Charge Pump Parameters," discloses an improved phase lock loop frequency synthesizer capable of handling both analog and digital transmission.

U.S. Patent 5,157,354 to Saiki et al., "Phase-Locked Loop IC Having ECL Buffers," discloses a phase locked loop IC comprising a voltage controlled oscillator which generates a clock signal in accordance with a control voltage.

U.S. Patent 5,216,302 to Tanizawa, "Reference Delay Generator and Electronic Device Using the Same," discloses a reference delay generator including a delay unit having a plurality of delay elements which are cascaded and respectively have variable delay times.

U.S. Patent Application Publication No. U.S. 2001/0013800 A1, Pub. Date: Aug. 16, 2001, to Wu et al., "Compensation Circuit for Low Phase Offset for Phase-Locked Loops," discloses a phase-locked loop circuit and method for providing for compensation for an offset.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
ERD-01-001	10/016,815
Applicant	
David Meltzer	
Filing Date	Group Art Unit
12/14/01	2631

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6215834	4/10/01	McCollough	375	375	8/4/97
	5963608	10/5/99	Casper et al.	375	373	6/26/97
	5886582	3/23/99	Stansell	331	1A	8/7/96
	5870002	2/9/99	Ghaderi et al.	331	17	6/23/97
	5838749	11/17/98	Casper et al.	375	376	6/5/95
	5822387	10/13/98	Mar	375	376	3/25/96
	5724007	3/3/98	Mar	331	1A	3/25/96
	5394444	2/28/95	Silvey et al.	375	374	7/12/93
	4499434	2/12/85	Thompson	331	17	7/19/82
	5359727	10/25/94	Kurita et al.	395	550	3/2/90
	5463329	10/31/95	Kawasaki et al.	326	77	4/8/94

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	"Phase-Lock Loop Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs," Nayan Patel, SCAA033A, Texas Instruments, March 1997.
	"Phase-Locked Loops for High-Frequency Receivers and Transmitters - Part 1," Curtin and O'Brian, Analog Dialogue, 33-3, 1999.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE JC17 FEB 26 2002 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
ERD-01-001	10/016,915
Applicant: David Meltzer	
Filing Date: 12/14/01	Group Art Unit: 2631

RECEIVED MAR 04 2002 Technology Center 2600

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	5,382,923	1/17/95	Shimada et al.	331	8	4/5/94
	5,570,042	10/29/96	Ma	326	63	1/3/95
	5,581,214	12/3/96	Iga	331	16	8/30/95
	5,793,225	8/11/98	Gerson	326	68	1/2/96
	5,905,386	5/18/99	Gerson	326	73	2/27/98
	6,246,294	6/12/01	Gai	331	57	2/12/99
	6,285,262	9/4/01	Kuriyama	331	25	6/29/99
	5,614,843	3/25/97	Mita et al.	326	73	1/5/96
	5,889,437	3/30/99	Lee	331	16	7/11/97
	6,111,469	8/29/00	Adachi	331	17	8/20/98
	4,736,167	4/5/88	Kojima et al.	331	17	6/23/86

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	The TQ8103 Clock + Data Recovery (CDR) product description manufactured by Triquint Semiconductor Inc. of a monolithic CDR IC.
	The AMCC S3040A Device Specification (April 2, 2000) of a clock recovery unit.

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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OIPE JC117 PATENT & TRADEMARK OFFICE FEB 26 2002

Docket Number (Optional)	Application Number
ERD-01-001	10/016,915
Applicant: David Meltzer	
Filing Date: 12/14/01	Group Art Unit: 2631

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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	4,818,950	4/4/89	Ranger	328	155	4/24/87
	5,151,665	9/29/92	Wentzler	331	8	2/7/91
	5,157,354	10/20/92	Saiki et al.	331	1A	11/27/91
	5,216,302	6/1/93	Tanizawa	307	603	9/18/91
Patent App. 2001	00 138 001 A1	8/16/01	Wu et al.	327	156	7/22/99

FOREIGN PATENT DOCUMENTS

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